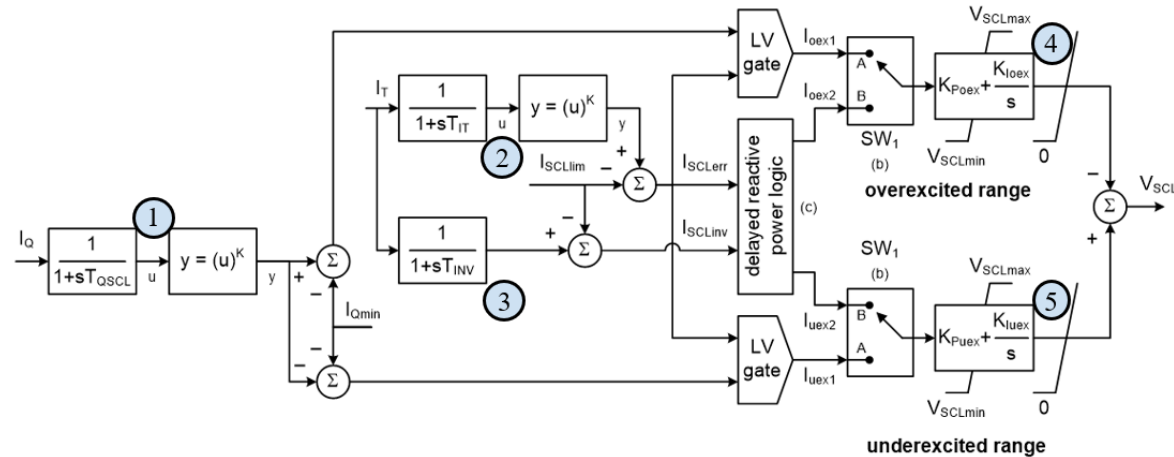


Stator Current Limiter SCL1C

Stator Current Limiter SCL1C IEEE Std 421.5-2016 Stator Current Limiter

States:

- 1 – IQ
- 2 – IT
- 3 – ITINV
- 4 – IntegratorIoex
- 5 – IntegratorIuex



footnotes:

- (a) The reactive current I_Q is defined in this model as the reactive power output of the generator (Q_T) divided by the magnitude of the terminal voltage (V_T). In other words, I_Q is positive for overexcited operation.
- (b) SW_1 is a user-selected option. When position A is selected, the SCL response is derived from the reactive current. When position B is selected, the SCL response is derived from reactive power.
- (c) The delayed reactive power logic uses user-selected parameters SW_2 , T_{DSCL} and V_{SCLdb} . It also uses the signals I_{SCLerr} and I_{SCLinv} shown in the block diagram, and the generator reactive power output Q_T :

```

IF [(SW2 = 0) and (ISCLerr > 0 for longer than TDSCL)] or [(SW2 ≠ 0) and (ISCLinv > 0)] THEN
  IF QT > VSCLdb THEN
    Ioex2 = ISCLerr
    Iuex2 = 0
  ELSEIF QT < -VSCLdb THEN
    Ioex2 = 0
    Iuex2 = ISCLerr
  ELSE
    Ioex2 = 0
    Iuex2 = 0
  ENDIF
ELSE
  Ioex2 = 0
  Iuex2 = 0
ENDIF

```